**IN THE CLAIMS:**

Please cancel claims 1, 6 and 28-30 without prejudice.

Please amend the claims as indicated below. Below are the amended claims in clean, unmarked format.

2. (Amended) The apparatus of claim 4 wherein the duty cycle correction circuit includes

a feedback path between an input and an output of the duty cycle correction circuit, the feedback path to control a delay of a circuit path in the duty cycle correction circuit to correct the duty cycle.

4. (Amended) An apparatus comprising:

a clock distribution network to distribute a clock signal on an integrated circuit chip;

a duty cycle correction circuit at a receiver in the clock distribution network, the duty cycle correction circuit to correct a duty cycle of a distributed clock signal received at the receiver; and

frequency multiplying circuitry coupled to the duty cycle correction circuit, the frequency multiplying circuitry to receive the distributed clock signal at an input and provide an output clock signal having a frequency that is a multiple of the distributed clock signal.

5. (Amended) The apparatus of claim 4 further including a smart buffer circuit coupled to the duty cycle correction circuit, the smart buffer circuit to provide for proper operation of the duty cycle correction circuit over a range of loads to be coupled to the duty cycle correction circuit.

7. (Amended) The clock distribution network of claim 8 wherein the clock distribution circuitry is further to distribute the global clock signal from the clock generation circuitry to a plurality of receiving points and wherein each of the plurality of receiving points is coupled to the duty cycle correction circuit.

8. (Amended) A clock distribution network comprising:

clock generation circuitry at a first location to generate a global clock signal;

clock distribution circuitry to distribute the global clock signal on an integrated circuit chip from the clock generation circuitry to a receiving point at a second, different location on the integrated circuit chip; and

a duty cycle correction circuit at the receiving point to correct the duty cycle of the distributed global clock signal received via the clock distribution circuitry,

wherein one of the receiving points further includes frequency multiplying circuitry coupled to the duty cycle correction circuit.

9. (Amended) The clock distribution network of claim 8 wherein the duty cycle correction circuit includes a feedback path to control a delay of an output clock signal.

11. (Twice Amended) The clock distribution network of claim 8 wherein the duty cycle correction circuit provides a corrected output clock signal having a substantially 50% duty cycle.

18. (Twice Amended) An integrated circuit chip comprising:

a clock generation circuit to provide a first clock signal having a first duty cycle;

a clock distribution network coupled to the clock generation circuit to distribute the first clock signal across the integrated circuit chip; and

a plurality of duty cycle correction circuits at receiving points in the clock distribution network, the duty cycle correction circuits to correct a duty cycle of distributed first clock signals at the receiving points.

31. (Amended) The apparatus of claim 2 further including:

a sense amplifier in the feedback path, the sense amplifier having a threshold substantially equal to one half of the supply voltage (Vcc) to be coupled to the duty cycle correction circuit.

33. (~~New~~ Amended) The apparatus of claim 32 wherein each of the reset path and the feedback path is coupled to control a variable delay element.

35. (Amended) The apparatus of claim 34 wherein the smart buffer includes

a first phase detector to detect a difference in delay between one of a rising or falling edge of the output clock signal and a corresponding edge of the reference signal, the first phase detector to provide a first reference control signal at a first output, the first reference control signal to control a delay of a first delay element in the duty cycle correction circuit to adjust the drive strength of the driver for a first value of an input signal to the duty cycle correction circuit.

36. (Amended) The apparatus of claim 35 wherein the smart buffer circuit further includes

a second phase detector to detect a difference in delay between a remaining one of a rising or falling edge of the output clock signal and a corresponding edge of the reference signal, the second phase detector to provide a second reference control signal at a second output, the second reference control signal to control a delay of a second delay element in the duty cycle correction circuit to adjust the drive strength of the output driver for a second value of the input signal to the duty cycle correction circuit.